UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,906,939 B2
DATED : June 14, 2005
INVENTOR(S) : Darrell Rinerson et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 3,
Line 36, in the "Brief Description of the Drawings", please replace the words "four layer of memory" with the correct words -- four layers of memory --.

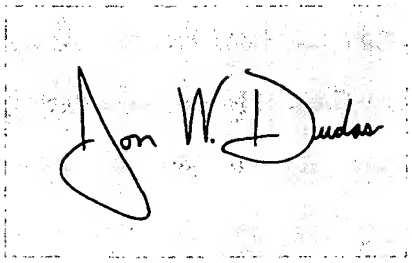
Column 16, line 61 through Column 17, line 3,
Please replace all instances of "x-direction conductive array layers" with -- x-direction conductive layers --; and replace all instances of "y-direction conductive array layers" with -- y-direction conductive layers --.

Column 17,
Line 4, please replace "x-direction conductive array layers" with -- x-direction conductive layers --.
Line 7, please replace all instances of "x-direction conductive array layers" with -- x-direction conductive layers --.
Lines 12-33, please replace all instances of "x-direction conductive array layers" with -- x-direction conductive layers --; replace all instances of "y-direction conductive array layers" with -- y-direction conductive layers --; and please replace all instances of "y-direction conductive array line" with -- y-direction conductive layer --.
Line 54, please replace "four memory cell array" with -- four memory cell arrays --.

Column 18,
Line 28, please replace "the re-writable is accessed" with -- the re-writable memory is accessed --.
Line 39, please replace "x-direction conductive array line" with -- x-direction conductive layer --; and replace "y-direction conductive array line" with -- y-direction conductive layer --.

Signed and Sealed this

Eighth Day of November, 2005



JON W. DUDAS
Director of the United States Patent and Trademark Office